EXPRESS MAIL LABEL NO. EV175409692US
DATE OF DEPOSIT: February 10, 2004

ABSTRACT OF THE DISCLOSURE

In one embodiment, an IC with an embedded processor core, peripheral devices, and associated multiple scan chains, is provided with microcode that implements an arithmetic pseudo-random number generator and an arithmetic deterministic test vector generator, when executed by the embedded processor core, generates 2-D pseudo-random and deterministic test vectors for testing the peripheral devices respectively. The IC is further provided with microcode that implements an arithmetic test response compactor, which when executed by the embedded processor core, compacts test responses of the peripheral devices into a signature. The IC further includes a test port register and microcode that implements a number of ABIST instructions.